The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte TAKAO TOI

Appeal No. 2006-0855
Application 09/505,429[1]

HEARD: April 27, 2006

Before JERRY SMITH, BARRETT, and SAADAT, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-22.

We reverse.

[1] Application for patent filed February 16, 2000, entitled "Image Processing System," which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Application 038970/1999, filed February 17,1999.

BACKGROUND

The invention relates to an image processing system that processes image data from a digital still or video camera. In the prior art, a general purpose CPU or wired logic processing device executed image processing, such as color separation processing or image compression processing, but CPU performance was often insufficient and incapable of parallel operation and dedicated wired logic devices took a long time to design and manufacture (spec. at 1-3). The invention uses a "field programmable gate array" (FPGA), which is a semiconductor device containing programmable logic components and programmable interconnects that can be dynamically ("on-the-fly") programmed by an "internal logic description" (or application program) written into the FPGA from a memory (spec. at 3). The FPGA performs image processing (e.g., image compression) during a time interval when the pixels are active and control processing (e.g., automatic white balance control processing, auto-focus control processing, or automatic lightness control processing) during a time interval when the pixels are not active, such as during a horizontal or vertical blanking interval (spec. at 4-5).

Claim 1 is reproduced below.

> 1. An image processing system provided with a field programmable gate array which is capable of altering an internal logic description, said description prescribing operation during an operating state, wherein an image processing method of said image processing system comprises:

executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;

executing digital control processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and

executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description;

wherein all operations necessary to perform said digital image processing and said digital control processing are performed in said field programmable gate array.

THE REFERENCES

The examiner relies on the following references:

Kolchinsky	5,301,344	April 5, 1994
Baxter et al. (Baxter)	5,486,853	January 23, 1996
Fukuoka	5,754,227	May 19, 1998

THE REJECTIONS

Claims 1-4, 7-14, and 17-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baxter and Kolchinsky.

Claims 5, 6, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baxter and Kolchinsky, further in view of Fukuoka.

We refer to the final rejection (pages referred to as "FR__") and the examiner's answer (pages referred to as "EA__") for a statement of the examiner's rejection, and to the brief (pages referred to as "Br__") and reply brief (pages referred to

as "RBr__") for a statement of appellant's arguments thereagainst.

DISCUSSION

Rejection and arguments

The examiner finds that Baxter discloses an image processing system having a processor 66 that executes digital image processing during an interval of active pixel and a processor 70 that executes digital control pre- or post-processing during an interval of non-active pixel (i.e., during the vertical blanking interval (VBI) of the analog signal) (FR3). The examiner finds that Baxter does not teach utilizing an FPGA for executing said image and control processing, but uses dedicated processors 66 and 70 (FR3). The examiner finds that Kolchinsky teaches that, conventionally, separate image processing operations require separate processors, and discloses a reconfigurable image processing system implemented by FPGAs which can be used to perform a variety of operations, so that processing algorithms can be changed easily and quickly (FR4). The examiner finds that Kolchinsky teaches image processing (e.g., image compression and color processing) and control processing (e.g., zooming/panning) (FR4). The examiner concludes that it would have been obvious to replace Baxter's separate processors 66 and 70 with Kolchinsky's reconfigurable FPGA "since Kolchinsky provides a much simpler and

more hardware-efficient system for effecting image and control processing" (FR4).

Appellant argues that "Kolchinsky does not disclose or suggest using an FPGA to perform digital control processing" and, therefore, one skilled in the art would not have been motivated to replace control processor 70 (which performs control processing) with an FPGA (Br6). It is argued that the reference to "zooming/panning" in Fig. 4 of Kolchinsky is not an example of digital control processing, but relates to manipulation of the image captured by the system (Br5). Appellant argues that Baxter does not disclose that processor 70 is used for image processing or that processor 66 is used for control processing (Br7). It is also argued that the camera head is separated from the main body and, therefore, to combine processors 66 and 70 it would be necessary to use a wired logic processing device, such an ASIC, instead of a general purpose CPU (Br7).

The examiner maintains that Kolchinsky discloses an FPGA to perform digital control processing (EA9). The examiner finds that Kolchinsky did not explicitly define the terms "zooming" and "panning" and these terms should be construed in accordance with their conventional usage, which refer to controlling the position of the camera lens and camera head--control functions (EA10). The examiner also finds that the "image acquisition" function

presumably refers to controlling the acquisition of an image, such as turning a camera on or off (EA10).

Appellant replies that the zooming/panning in Fig. 4 of Kolchinsky can refer to manipulation of an image and not control of the camera as found by the examiner (RBr2). It is also argued that the examiner's presumption that image acquisition is a control operation, such as turning a camera on or off, is pure speculation and a more reasonable reading is that the image is acquired from the image data bank (RBr2-3).

The examiner additionally states (EA10-11):

> Also, regardless of whether Kolchinsky discloses his FPGA performing "digital control processing," the combination of Baxter and Kolchinsky should still be valid. Baxter discloses performing the necessary digital image and digital control processing, and Kolchinsky was only relied upon to show that it was obvious and advantageous to replace Baxter's separate processors with a single FPGA. In general, FPGAs are multi-purpose, reprgorammable [sic] processors that are capable of performing virtually any operation or algorithm that can be executed by a dedicated processor. Even if Kolchinsky did not expressly disclose performing digital image and control processing with an FPGA, that omission would not negative the fact [that] FPGAs are capable of performing such processing, nor should it render the proposed combination invalid.

The closest argument we find in response is that Kolchinsky discloses merging multiple digital image processors, but it does not disclose merging digital control processors with digital image processors (RBr3). "Because the processing requirements for image processing and control processing are different,

Kolchinsky would not suggest to one skilled in the art to combine processors 66 and 70 [in Baxter] into one FPGA" (RBr3-4).

Analysis

Baxter discloses a video camera system including an electronic camera head 12 where horizontal and vertical synchronizing signals and pixel clock signals are generated and transmitted along with analog video signals generated by a solid-state video imager to a remote host processor 14. The electronic camera head 12 is connected via an electrical cable 13 to the remote host processor 14, such as a video card in a host personal computer 16, having digital signal processing circuitry for processing the analog video signals. The analog signals are converted to digital video signals and then processed by the digital signal processing circuitry. See col. 2, lines 25-34; Figs. 1, 2, and 8. The advantages are that the "intelligence" processing is located within the remote host processor with only the analog processing needed to prepare the raw analog signals for noise-free transmission remaining in the camera head, and the quality of the raw video image data is maintained and is not lost during conversion/reconversion from analog to digital and back into analog format (col. 2, lines 42-51). Furthermore, the cost and size of the camera head and the electrical cable can be smaller (col. 3, lines 1-24). The remote host processor 14

contains a digital camera processor 66 which provides image processing on digital data (col. 7, lines 12-34). In one embodiment, a processor 70 can be located in the camera head 12. Control signals are sent from the host computer 16 through the remote host processor 14 along conductor 50 during the vertical blanking interval (VBI) portions of the analog video signal (col. 7, lines 44-51). The control signals may be used to vary the incident light exposure by controlling an iris in the lens system, or to control the position of the lens in relation to the CCD for focusing or zooming, or other control functions (col.7, lines 51-61). The processor 70 may transmit data information back to the computer 16 during the VBI (col. 7, lines 62-67; col. 8, lines 12-19).

The examiner's findings that Baxter teaches performing image processing during the interval of an active pixel and performing control processing (pre-processing or post-processing in the terminology of claim 21) during an interval of non-active pixel (i.e., during the VBI) are reasonable and are not challenged by appellant. Since the bi-directional signals to and from the control processor 70 take place over the conductor 50 during the VBI, it is possible that image processing is still taking place during the VBI and that control processing in response to the control signals takes place continuously even during a period of the active pixel; i.e., it is not clear that the image processing

and control processing functions in Baxter are mutually exclusive in time. However, this possibility has not been argued by appellant. The question is whether one of ordinary skill in the art would have been motivated to replace the separate processors 66 and 70 with a reconfigurable FPGA.

Kolchinsky discloses a reconfigurable sequential processor having an address generator 22 and arithmetic unit 26, which may be implemented with field programmable gate arrays (col. 6, lines 51-54). A list of available processes for which the system may be reconfigured is shown in Fig. 4 (col. 4, lines 40-42).

We agree with appellant that Kolchinsky does not teach or suggest control processing. Kolchinsky describes only a computer containing the reconfigurable sequential processor and does not show the processor in the environment of a camera or other equipment that is controlled. One of ordinary skill in the art would interpret the "image acquisition" and the "zooming/panning" in Fig. 4 as image processing operations in the absence of any disclosure of controlling external equipment. Nevertheless, this does not end the obviousness inquiry because the examiner maintains that the claimed subject matter would have been obvious because Kolchinsky is only relied upon to show that it was obvious and advantageous to replace Baxter's separate processors with a single FPGA. Appellant argues that Kolchinsky discloses merging multiple digital image processors, but it does not

disclose merging digital control processors with digital image processors (RBr3) and "[b]ecause the processing requirements for image processing and control processing are different, Kolchinsky would not suggest to one skilled in the art to combine processors 66 and 70 [in Baxter] into one FPGA" (RBr3-4).

While reconfigurable FPGAs, which swap the internal logic descriptions to perform different functions, were well known as evidenced by Kolchinsky, we have trouble seeing why or how the processors 66 and 70 would be replaced by a single FPGA which performs both image processing and control processing functions. Control processor 70 is in the camera head 12 and image processor 66 is in a remote host processor 14; furthermore, the control processor 70 receives its control signals from the host computer 16 and transmits signals back to the host computer 16 through the cable 13. First, since the control processor 70 performs a number of different functions (e.g., controlling an iris in the lens system, focusing, zooming, panning, tilting, see col. 7, lines 51-59) and the image processor 66 performs a number of different functions (e.g., color stripe demodulation, automatic lighting balance, etc., see col. 7, lines 11-33), it would seem more logical to replace each processor with a FPGA, each to perform either control or image processing functions, rather than combine both processors into a single FPGA. If Kolchinsky did teach both control and image processing in the

same FPGA, the examiner's rejection would have been much stronger. Second, since the processors in Baxter are separated by a cable, it is not a mere matter of substituting a single FPGA for the multiple processors; it has not been explained why one skilled in the art would have been motivated to replace processors at different ends of the system with a single FPGA. Third, it is noted that the bi-directional control and information signals to/from the control processor 70 come from the host computer 16 and it is not clear how the examiner specifically proposes to modify Baxter to have a single FPGA, except in some general conceptual way. Although these questions are not raised by appellant's arguments, we conclude that the examiner has failed to establish a prima facie case of obviousness. For these reasons, the rejection of claims 1-4, 7-14, and 17-22 over Baxter and Kolchinsky is reversed. Fukuoka does not cure the deficiencies of Baxter and Kolchinsky and therefore the rejection of claims 5, 6, 15, and 16 is reversed.

REVERSED

JERRY SMITH)
Administrative Patent Judge)
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LEE E. BARRETT) BOARD OF PATENT
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) AND
) INTERFERENCES
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